Epitaxial Growth of III–V Nanowires on Group IV Substrates

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Abstract

Semiconducting nanowires are emerging as a route to combine heavily mismatched materials. The high level of control on wire dimensions and chemical composition makes them promising materials to be integrated in future silicon technologies as well as to be the active element in optoelectronic devices.

This article reviews the recent progress in epitaxial growth of nanowires on non-corresponding substrates. We highlight the advantage of using small dimensions to facilitate accommodation of the lattice strain at the surface of the structures. More specifically, we will focus on the growth of III–V nanowires on Group IV substrates. This approach enables the integration of high-performance III–V semiconductors monolithically into mature silicon technology, since fundamental issues of III–V integration on Si such as lattice and thermal expansion mismatch can be overcome. Moreover, as there will only be one nucleation site per crystallite, the system will not suffer from antiphase boundaries.

Issues that affect the electronic properties of the heterojunction, such as the crystallographic quality and diffusion of elements across the heterointerface, will be discussed. Finally, we address potential applications of vertical III–V nanowires grown on silicon.

Introduction

"Epitaxy" is derived from the Greek word meaning "ordered upon" and describes the crystalline deposition of material on a substrate with identical lattice structure and orientation. For heteroepitaxial growth, materials with different lattice parameters are combined. If the lattice mismatch between the deposited film and the substrate is large, typically a few percent, undesirable misfit dislocations can be incorporated near the interface. Alternatively, adlayers may form three-dimensional nuclei to release the strain in order to minimize the energy in the system, at the cost of creating more surface.

With the development of the vapor–liquid–solid (VLS) wire growth method in 1964,[1] it has become possible to vary the chemical composition (and inherent lattice parameters) within a nanowire. With this method, thin semiconducting nanowires are grown from a catalytic metal particle. The small diameter (typically some tens of nanometers) results in effective strain release, circumventing the usual requirement of lattice matching. Several groups have recently shown that such heteroepitaxial junctions can be defined in nanowires in the longitudinal (axial)[2–6] direction as well as in the radial[6–11] direction for different III–V compound semiconductors and for the Si/Ge system. These different materials can have a substantial lattice mismatch, and the crystal lattices will be elastically deformed near the heterointerface. Such crystal deformations can be relieved at the surface for small enough wire diameters. If the lattice strain is totally accommodated by elastic deformations, the introduction of misfit dislocations at the heterointerface will be avoided. Such strain relief in, for instance, a heterostructured InAs/InP (~4% mismatch) nanowire has been supported by a detailed analysis of the electrical characteristics.[12,13] Importantly, this method allows us to combine heavily mismatched semiconductors, maintaining perfect crystallinity.

This concept of strain engineering can be extended to grow nanowires on a substrate with different lattice parameters, or in other words, to have the heterointerface at the nanowire/substrate junction. Epitaxy of VLS-grown (sub)micrometer-sized whiskers on corresponding bulk substrates was pioneered in the 1970s by Wagner[14] and Givargizov[15–17] for the Si/Ge system, and Hiruma[18,19] investigated VLS growth of compound semiconductor nanowhiskers in the early 1990s. In recent years, Ge nanowires have been heteroepitaxially grown on silicon,[20,21] GaN and ZnO nanowires on oxidic substrates,[22–24] and ZnSe on GaP.[25] More recently, growth of III–V nanowires on silicon[26–28] and germanium[29] substrates has been reported.

In this context, the nanowire epitaxy approach may be interesting for the monolithic integration of III–V semiconductors into silicon technology. This combines the best parts of two worlds: the superior electronic properties of the III–V semiconductors with the highly advanced and relatively inexpensive silicon process technology. Most of the III–V materials intrinsically have higher electron mobilities and a direct bandgap, whereas silicon has a higher thermal conductivity and favorable mechanical properties as compared with the III–V substrates.

This article highlights recent developments that have been made with regard to the structural and chemical characterization of epitaxial III–V nanowires on silicon or related substrates.

Nanowire Epitaxy

Nanowires grown by the VLS mechanism are nucleated from a nanometer-sized metal seed or catalyst particle that collects the precursor material from the vapor phase, establishing local supersaturation. There are a few examples showing that the metal particle acts as a catalyst for the decomposition of the precursor molecules.[6,30] A vapor pressure of the precursor components can be created by means of molecular-beam epitaxy (MBE),[31–34] metalorganic vapor-phase epitaxy (MOVPE)[14–19] and related techniques,[35] pulsed laser ablation,[36–39] or by simple evaporation of the precursor material.

When supersaturation has been reached, crystalline material precipitates underneath the metal particle. In order to enable epitaxial growth of a nanowire, it is of crucial importance to have a clean and crystalline substrate surface. Methods to clean Si substrates are well established, and an etching step with hydrofluoric acid is almost always included. The catalytic metal particles are deposited directly after substrate cleaning. So far, Au has mainly been used as the active particle, but alternative metals,[14,16,30,38] oxides,[40] and silicides,[41] being compatible with standard silicon processing, have been used to some extent. Importantly, any exposure to air affects the epitaxy, since Au catalyzes the oxidation of Si; an SiO_2 layer tens of nanometers thick forms on top of the Au particle within days at room temperature.[42] Alternatively, Si samples provided with a thin Ge layer or bulk Ge samples have been used,[29] since any germanium oxide is readily desorbed by a mild *in situ* thermal treatment.

Scanning electron microscopy (SEM) can give a first indication of nanowire epitaxy. Epitaxial growth results in alignment of the nanowires in specific directions determined by the crystal symmetry of the substrate. However, orientation of one-dimensional structures can also be obtained during growth by other mechanisms, such as interaction with external fields[43] or with a gas flow.[44,45] In general, the III–V wires tend to grow in the [111]B direction,[16,18] which means that the wire crystal is terminated at the wire/catalyst interface by a Group V plane. Therefore, vertical growth can be induced on ⟨111⟩B-oriented III–V substrates. We should note, however, that the elemental semiconductors, such as silicon, are not polar, and all {111} facets are chemically equivalent. When growing III–V wires on a silicon (111) substrate, non-vertical wire growth is expected if the growth is nucleated from {111} facets other than those at the substrate surface. These other planes become available by alloying of the Au catalyst particle with Si prior to growth;[27,28] in other words, the Si surface is etched, creating the other {111} facets from which the wire growth can now be initiated. Similar alloying has been observed for Au particles on InP(100) substrates, which resulted in non-vertical growth directions.[46] Such alloy etching has not been observed with Au particles on Ge substrates.

This means that the III–V wires can grow in the four ⟨111⟩ directions on a (111)-oriented Si substrate. This has, for instance, been observed for the growth of InP on (111)-oriented silicon substrates (see Figure 1a)[27] having a mismatch of 8.1%. There are three clearly noticeable orientations with in-plane components parallel to the sides of an equilateral triangle. Some wires are oriented perpendicular to the surface, and in this top view they appear as small bright spots. The observed preferential orientations correspond to the four ⟨111⟩ directions typical for a (111)-oriented crystal: one orientation perpendicular to the surface and three orientations forming a 19° angle with the surface, having in-plane components at 120° from each other (see Figure 1b).

Besides growth from the other {111} facets, there is an additional mechanism to induce non-perpendicular growth, which is related to the lattice mismatch between the wire and substrate. For systems with a small lattice mismatch, samples have been prepared with mostly vertical wires, such as GaP/Si (0.4%), and GaAs/Ge (0.1%), as shown in Figures 1c and 1d. For systems with an intermediate mismatch, such as InP/Ge (3.7 %) and GaAs/Si (4.1%), the four typical ⟨111⟩ directions are equally

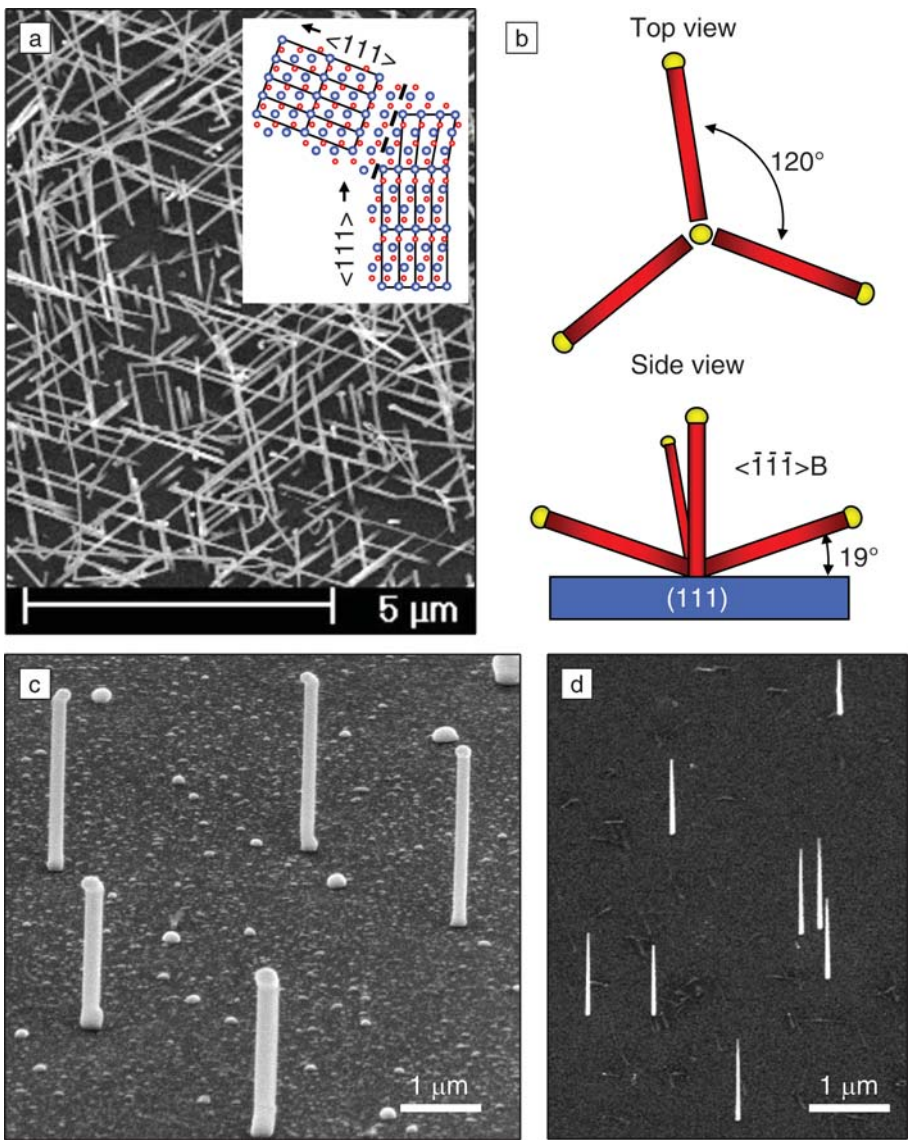

Figure 1. (a) Scanning electron microscopy image (top view) of InP wires grown by metal-organic vapor-phase epitaxy on a Si(111) substrate. Inset in (a) shows the mechanism to relieve compressive strain in the nanowire base by a change into another ⟨111⟩ growth direction without a rotational twin dislocation. (b) Expected wire orientations on a (111)-oriented silicon or germanium substrate. (c), (d) SEM images (side view, 30°) of (c) GaP wires grown by laser ablation on Si(111) and (d) GaAs wires grown by MOVPE on Ge(111).

abundant; for the most heavily mismatched systems, InP/Si (8.1%) and InAs/Si (11.6%), the non-perpendicular growth directions dominate. This shows that lattice strain has a major effect on the wire orientation. The residual compressive strain in the base of the wire can be relieved by a change into another ⟨111⟩ growth direction, as shown schematically in the inset of Figure 1a. We studied these strain effects in more detail,[27–29] and the results will be discussed later in the article.

Structural Characterization of Wire Ensembles

The fact that nanowires have well-defined orientations consistent with the substrate's crystal symmetry is a clear indication of epitaxial growth. X-ray diffraction (XRD) and cross-sectional transmission electron microscopy (TEM) are the established techniques to substantiate this. We studied the crystallographic relation between the substrate and a large number of nanowires by XRD pole figure measurements (Figure 2a).[27,29] Pole figures were measured for the (111) reflections of the substrate and the wires. In the reference pattern of the silicon substrate (Figure 2b), (111) spacings were found at four orientations typical for a (111)-oriented single crystal. One set of reflections is in the center of the pole figure, corresponding to the substrate normal; the other three sets have an in-plane angle of 120° with respect to each other (these orientations are reflected by the wire orientations as observed with SEM).

The pole figure for InP wires grown by MOVPE on Si(111) is shown in Figure 2c. The signals associated with the majority of the InP wires, labeled A in Figure 2c (i.e., about two-thirds of the total signal), match the pole pattern of the substrate, providing an unambiguous signature of heteroepitaxial growth. With such pole figures, we confirmed the epitaxial relation between a range of III–V nanowires such as GaAs, InP, and InAs with the Si(111) substrate.[27] The difference in lattice spacings for the GaP/Si system was too small to be resolved in the pole figures.

The most commonly found crystal defects in all types of nanowires are rotational twin dislocations, which occur specifically around a ⟨111⟩ axis.[14] In terms of electron wave function propagation, a twin behaves as a junction of two essentially different materials, and electrons can scatter at these interfaces.[47] The observed twin density in nanowires seems to be a function of growth temperature and wire diameter and strongly depends on the material system. Typically, the twin density observed is much lower in wires

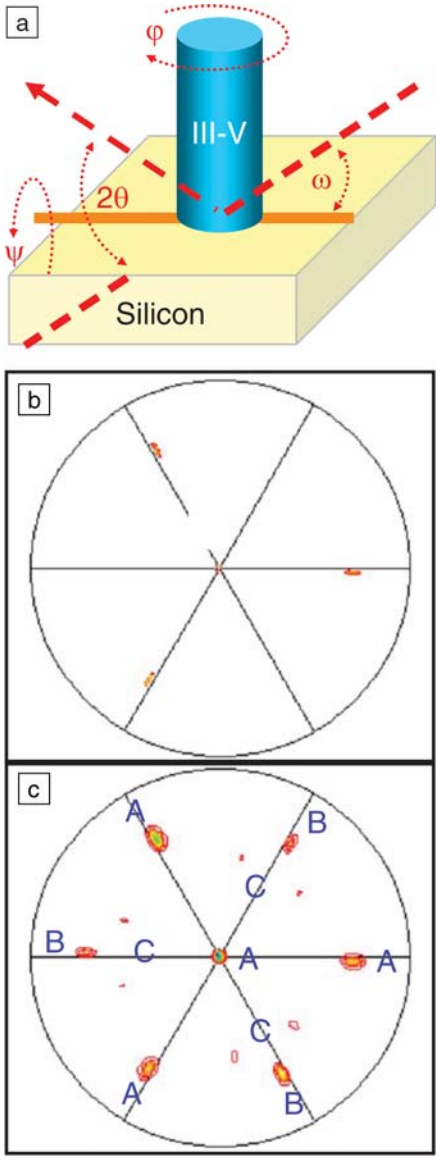

Figure 2. X-ray diffraction pole measurements on InP wires grown on Si(111). (a) Schematic illustration of the experimental geometry. To record the pole figure, the detector was set at a 2θ angle corresponding to one of these lattice spacings, and the substrate was rotated continuously around φ and stepped around Ψ. (b) Pole figure of the Si(111) reflections of the Si(111) substrate. (c) InP(111) reflections originating from the wires. Note the square root intensity scale in these plots. See text for discussion.

grown epitaxially on germanium and silicon than in wires grown on silicon oxide.

With x-ray pole measurements, it is possible to investigate the twin density for a large ensemble of wires. For example, the three spots in the pole figure (labeled B in Figure 2c) that have a 180° in-plane rotation with respect to the peaks from the epitaxial wires arise from wires that have a rotational twin dislocation around the substrate-surface-normal vector. The twin boundaries can be in the wire or at the wire/substrate interface. An example of such a twin boundary at the heterointerface is indicated by the white dotted line on the TEM cross section in Figure 3b.

The small signals appearing closer to the center of the pole figure (labeled C in Figure 2c) originate from wires that have grown in one of the non-perpendicular ⟨111⟩ directions, having an angle of 19° to the surface, and that have a twin dislocation orthogonal to their longitudinal axis. The fact that the mirrored orientations give a much smaller signal than the orientation identical to the substrate reveals that the density of twinning defects in the wires is very low (one or two per wire).

Interface Characterization at the Single-Wire Level

We have investigated the wire/substrate interface of individual wires in great detail by TEM.[27–29] For this study, vertical cross sections were sliced with a focused ion beam (FIB) and thinned by argon-ion milling. To provide mechanical support during this process, the wires were embedded in a microns-thick silicon oxide layer deposited by the spin-on process or by plasma-enhanced chemical vapor deposition (PECVD). Figure 3a shows an overview of a cross-sectional TEM image of a GaP wire grown on a Si(111) substrate. Figure 3b shows a high-resolution image of the wire/substrate interface. The lattice planes continue from the substrate into the nanowire, showing the epitaxial relation. However, the wire/substrate interface has a typical roughness of ~5 nm, which is unacceptable for applications in which the heterojunction plays a crucial role.

This roughness is a direct result of the Au/Si alloy formation[27,28] and the Au-catalyzed oxidation of Si at ambient conditions. Si atoms from the substrate diffuse through the Au particle to the Au/air (or Au/oxide) interface, where they react with oxygen to form a SiO_2 layer.[27] The SiO_2 on top of the Au particle is removed by HF etching just before the sample is inserted into the growth chamber. When the III–V precursors are introduced and absorbed by the particle, the Si that is still left in the particle is precipitated. This Si precipitation partially replenishes the etched pit (the other part has been oxidized and removed), and the rest is filled up with III–V material, resulting in a rough interface.

Such a rough interface has never been observed for InP wires grown on a Ge(111)

surface (3.7 % mismatch),[29] although the Ge concentration (28%) in the eutectic Au-Ge mixture is even higher than the Si concentration (18.6%) in the Au-Si system.[48]

A typical TEM image of an InP wire grown on Ge(111) is shown in Figure 4a. The flatness of the InP/Ge interface shows that uptake of substrate material to form the eutectic during sample heating and the subsequent precipitation is not the main origin for the surface roughening. This confirms that the rough wire/Si interface is mainly induced by the Au-catalyzed oxidation of Si at ambient.[28,42]

The InP/Ge epitaxy was investigated in more detail by taking the fast Fourier transformation (FFT) of the TEM image of the InP/Ge interface (see Figure 4b).[29] Double spots were observed, corresponding to the InP and Ge reciprocal lattices along the [011] zone axis. The lattice spacings corresponding to the InP wire, as extracted from the FFT pattern, are 0.5% lower than the literature values for InP.[49] This shows that for this wire, the InP lattice is almost but not fully relaxed within a few nanometers from the Ge substrate. High-resolution XRD measurements revealed that the crystal lattice parameters of the bulk of the wires correspond to the literature values. In addition, diffraction measurements have shown that the crystal lattice orientation of these wires is identical (±0.09°) to that of the substrate.[29]

In addition to crystal defects, diffusion of atoms across the interface may affect the electronic properties of the wires or of the active areas defined underneath the wires. Group III elements (In, Ga) are *p*-type dopants for Si and Ge, whereas the Group V elements (P, As) induce *n*-type doping. For certain applications, a low resistive substrate/wire contact is essential, and the interdiffusion could be employed to obtain highly doped regions close to the interface. On the other hand, the diffusion of species across the interface might be suppressed by a blocking layer to avoid degradation of highly advanced electronic structures.

The interdiffusion has been studied by TEM with energy dispersive x-ray analysis (EDX).[28] EDX line scans were taken across the interfaces, as indicated by the red line in Figure 3a. The heterointerface is in the range of x = 10–15 nm for GaP/Si (blue shaded area in Figure 3c) and around x = 70 nm for InP/Ge (blue shaded area in Figure 4c). The line scans for GaP/Si and InP/Ge show that both Group III and V elements diffuse into the substrate to at least some tens of nanometers below the substrate surfaces. For the GaP/Si system, we consistently observed[28] a slightly higher Ga than P concentration in the Si, whereas for InP/Ge, the P concentration in the Ge substrate was significantly higher than that of In. These trends are consistent with the solid solubilities of these elements in Si

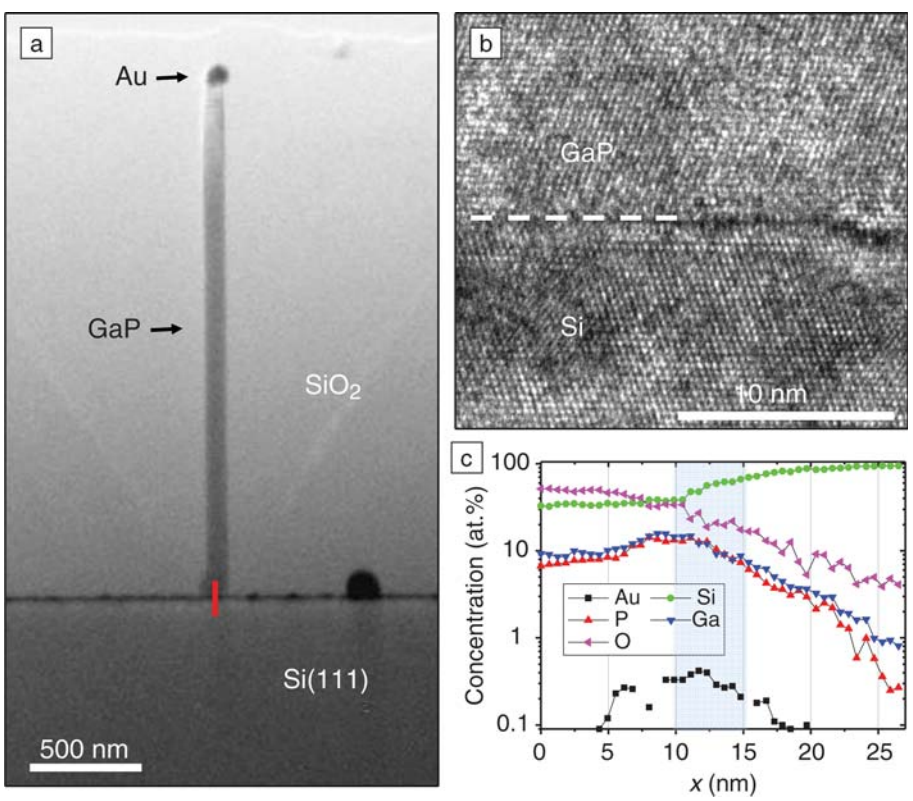

Figure 3. (a) Cross-sectional transmission electron micrograph of GaP wire on Si(111). The red vertical line signifies the position of the energy-dispersive x-ray line scan. (b) High-resolution image of the GaP/Si interface. The white dotted line indicates the position of the heterointerface and a twin boundary. (c) EDX line scan across the GaP/Si junction. The blue shaded area indicates the position of the heterointerface.

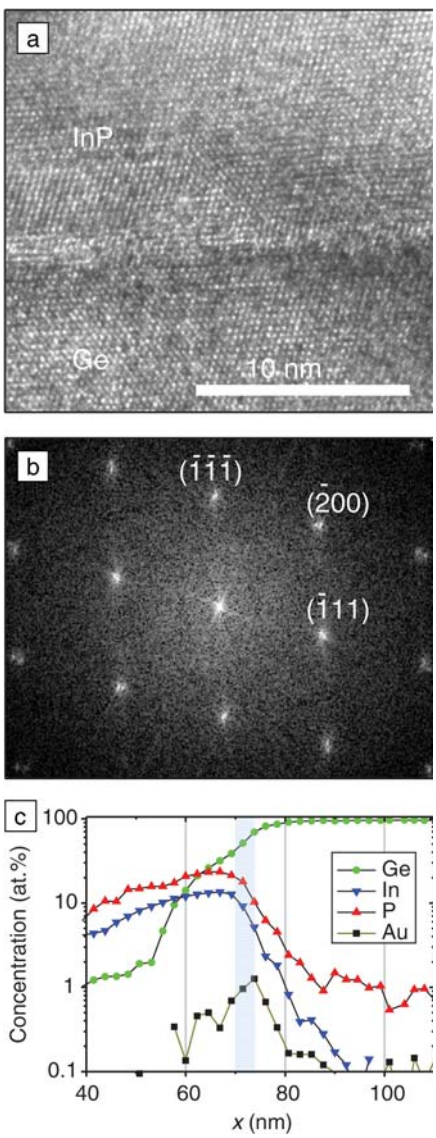

Figure 4. (a) Cross-sectional transmission electron micrograph of an InP nanowire/Ge substrate interface. (b) Fast Fourier transformation of the image shown in (a). (c) Energy-dispersive x-ray line scan across the InP/Ge junction. The blue shaded area indicates the position of the heterointerface.

and Ge.[50] Within the detection limit of EDX (0.2%), we could not detect any Au contaminant from the catalyst particle in the Si and Ge substrates nor in the nanowires. A small amount of Au was detected close to the interface. This signal originates from particles that have not initiated wire growth after breaking up the thin Au film.[28]

Issues at the Heterointerface

The crystallographic quality of the heterointerface might be of crucial importance for certain applications. Crystal imperfections at the interface can be induced by the polar/nonpolar nature of the materials and by the lattice mismatch.

Regarding growth of polar III–V semiconductors on a nonpolar elemental semiconductor, such as Si or Ge, nucleation can occur with either the Group III or the Group V element, resulting in opposite polarity. When two nuclei having opposite polarities merge, an antiphase boundary (APB) is formed. Alternatively, when the surface is uniformly covered with one of the precursor elements, APBs can still be formed at monoatomic steps on the substrate surface.[51] We stress here that APBs have not been observed in any of the nanowires. This could be explained by the growth being initiated from a single nucleation site per wire.

Any lattice mismatch will induce strain near the heterointerface. Obviously, wires are not constrained like thin films, allowing elastic deformation of the lattice parallel to the interface, relieving the epitaxial strain to some extent. Detailed analysis of high-resolution TEM and x-ray diffraction has shown that the wire/substrate interface is practically free of defects for wire/substrate materials combinations such as GaP/Si, GaAs/Si, GaAs/Ge, and InP/Ge, which have a lattice mismatch up to 4% and a wire diameter typically around 20 nm. For systems with a larger mismatch, such as InP/Si and InAs/Si, epitaxial growth has been demonstrated by the use of XRD, but high-resolution TEM reveals that strain-induced defects and kinks are present near the interface. For instance, InAs wires grown on Si(111) contain a complex pattern of twin boundaries at their bottom part that are oriented parallel to various {111} planes, resulting in a multiple twinned lump of material from which a single wire emerged, growing along its ⟨111⟩ axis. Due to the many twins separating the wire from the substrate, the long wire axis is not always exactly parallel to one of the substrate ⟨111⟩ vectors.

For a number of InP wires grown on Si(111), we observed a change into another ⟨111⟩ growth direction as a mechanism to relieve the lattice strain, as indicated in the inset of Figure 1a.[27] Often, such a change was not induced by a twin defect, implying that the growth is continued into a ⟨111⟩ direction with opposite polarity to that of the vertical part.

It seems that a maximum mismatch of about 4% is allowable for the typical wire dimensions without suffering from defects and kinking. An obvious way to integrate heavily mismatched materials into silicon is to engineer the lattice constant within the wire. A gradual increase of the lattice mismatch with respect to silicon can, for instance, be realized by starting with a GaP (0.4%) segment at the base of the wire, followed by sections of GaAs (4.1%), InGaAs, and InAs (11.6%).

Applications and Challenges

Monolithic, or single-crystalline, integration of optically active and high-mobility semiconductor nanowires into the mature silicon technology not only could boost the performance of existing devices, but moreover introduce new functionalities. Epitaxial nanowires on (relatively cheap) silicon substrates open up promising applications in the fields of electronics, optoelectronics (light emission[5,19] and detection[52]), sensors (gas and bio sensors[53]), energy scavenging (thermoelectrics[54] and solar cells[55]), and field emission.[17] For instance, nanowire-based *p*–*n* diodes electronically integrated in the silicon circuitry could enable fast optical interchip communication or could distribute and sense the chip's clock frequency optically. Optical signals do not suffer from resistive delays as in electronic circuits, and higher frequencies may become available. So far, there are just a few reports showing deliberate *n*- and *p*-type doping of III–V nanowires,[5,19,56,57] and an effort should be focused toward obtaining quantitative control of doping levels in the wires.

The possibility of engineering the electronic structure within a nanowire and at the nanowire/substrate junction in combination with a vertical geometry allows optimization of already existing devices, such as a field-effect transistor (FET).[58] For instance, InAs is a very interesting material, since it has a high electron mobility and it tends to form "ideal" ohmic contacts[59,60] to many metals. The highest reported values for the electron mobility in InAs wires (up to 10,000 $cm^2/V\,s$)[61] are still below that of the bulk material (33,000 $cm^2/V\,s$). The carrier mobility in wires is most probably limited by surface scattering, which could be suppressed by radial overgrowth of the core with a wide-bandgap semiconductor or by an organic capping.[62] In addition to the freedom of choice of material, a vertical geometry facilitates a wrap-around gate configuration, increasing the electrostatic coupling of the gate to the channel. A vertical FET device with a high-mobility channel and a gate-around geometry, as shown in Figure 5, is expected to show an enhanced transconductance.[58] Several groups have recently shown vertical FET devices with promising characteristics.[61,63–65] However, device performance needs further improvement in order to be able to contribute to current-day nanoscale CMOS devices.

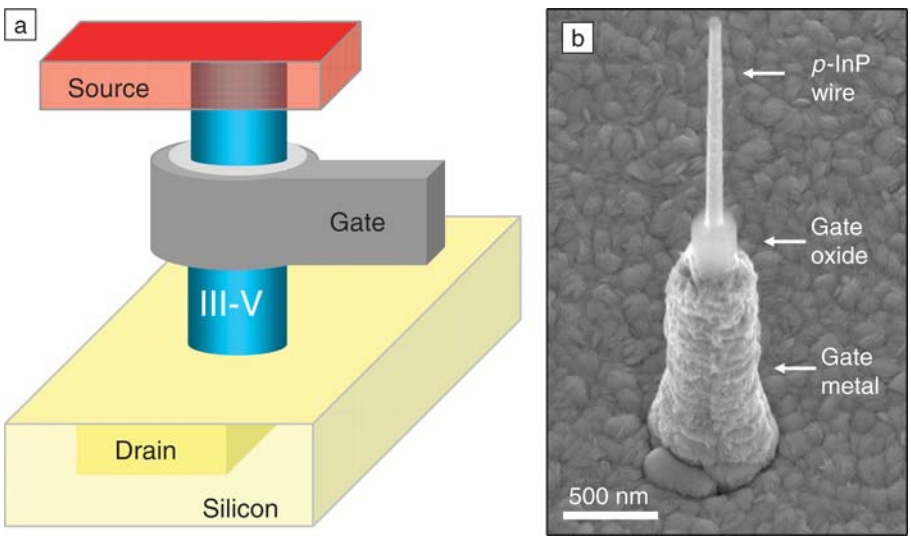

Figure 5. (a) Schematic illustration of a vertical nanowire transistor. The active channel is a III–V nanowire epitaxially connected to the silicon substrate, and the gate is wrapped around the channel. (b) Scanning electron micrograph (side view, 30°) of a nearly finished vertical device consisting of a p*-type InP wire covered with gate oxide and gate metal.*

Great progress has been made over the last few years in understanding and controlling nanowire growth and device fabrication. Nanowire heteroepitaxy represents an important step toward the final goal of bringing new materials and novel device layouts into silicon-based integrated circuits.

From a technological point of view, an important issue that still remains to be addressed is the vertical growth of III–V wires on currently used Si(100) substrates. Therefore, the nanowires must grow in the [100] direction. Considering the III–V materials, InAs[59,66] and InP[46] wires have been grown in this direction using homoepitaxy.

Finally, epitaxial growth of nanowires on silicon enables electrical characterization of the junction between heavily mismatched semiconductors. So far, only a few papers have reported preliminary data on the electronic properties of the III–V/Si wire/substrate junction.[27,29] The effects of polar/nonpolar interfaces and strain on the electronic properties are important for any application, and these have to be properly assessed.

Acknowledgments

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